MPM-06:000672 Uen Rev A

Performance Improvements for OEM System Designers - A Digital Control Case Study

September 2006

Technical Paper

Digital control can be used as an enabling technology to offer cost, reliability and power density improvements to the end user with no additional design effort required from the OEM system designer.

ERICSSON

TAKING YOU FORWARD

Contents

1 Executive summary

Digital control techniques can be applied at several points within a power system, both internal to power converters and at the system level for purposes of implementing control and monitoring functions. This paper elaborates on the former situation. It compares the effects at the system level of implementation of control functions internal to a dc/dc regulator with digital techniques vs. the more traditional analog approaches. With either of the approaches considered in this comparison, the end user of the regulator may treat the device in a traditional way without any need for digital techniques at the system level. The comparison is done by means of a case study using an actual production product with only the minimal required changes to the power train so that the effects of the control system implementation are highlighted. Some of the areas of interest in the comparison are electrical performance including efficiency, parts count, power density, cost and reliability. The comparison is done from an end-user's perspective rather than focusing on benefits to the regulator designer.

The power module used in the case study comparison is an Ericsson PMH8918L Point of Load (POL) regulator. This is an 18 amp non-isolated synchronous buck regulator with a programmable output voltage and a nominal 12 V input voltage. Most of the power train components were kept common between the analog and digital control designs, as described later. Electrical performance parameters were measured directly on the two designs. Calculations were used to estimate the differences between the regulators for parameters related to the respective parts counts of the two approaches.

The comparison results can be summarized as follows:

- The electrical performance, including efficiency, of the digitally controlled regulator is equal to or better than the analog version.
- The digital solution results in more than a 60% reduction in parts count. This increased integration will reduce the cost of the regulator.
- The reduced parts count results in a reduction in required real estate for the regulator circuitry. This can be used either to reduce the size of the device or to increase the power output within the present size envelope.
- The reduced parts count will increase the predicted reliability.

In conclusion, digital control can be used as an enabling technology to offer cost, reliability and power density improvements to the end user with no additional design effort required from the OEM system designer.

2 Test Configuration and Conditions

An Ericsson PMH8918L non-isolated POL regulator was selected as a baseline for the comparative study of differences between analog and digital control. This regulator has the following basic specifications:

- Output Current: 18 A
- Topology Synchronous Buck
- Control Traditional Analog PWM
- Input Voltage 10.8 to 13.2 V
- Output Voltage 1.2 to 5.5 V (user programmable)
- Switching Frequency 320 kHz
- Dimensions 38.1 x 22.1 x 9.0 mm (1.50 x 0.87 x 0.35 in)

The output voltage was adjusted by means of a resistor between the Vadj pin and ground. The remote sense pin was tied to the output pin (local sensing). This device was selected because it fits into a very popular voltage and current range for POL regulators and should provide useful data for a wide range of customers. It should be noted that while Ericsson expects that the conclusions shown in this paper should apply over a fairly broad range of operating currents and power modules, the testing to date was only done on a small group of samples of this specific regulator device.

The digital control implementation is based upon the ZL2005 chip developed by Zilker Labs, Inc.. The PCB has the same area as the PCB used in the PMH8918L. The switching frequency of this digital implementation is 333 kHz, very similar to that of the analog regulator. To obtain the most objective comparison, the power train components used in both versions were kept the same except as noted below.

The PMH8918L uses a set of Renesas FETs for the high side and low side switches. The digital control implementation was made with the same Renesas FETs. These test results are labelled as “Digital Renesas”. In order to make a small test of the “Efficiency Optimized Driver Dead time Control” (see section 5.12 in the referenced Zilker Labs datasheet) capabilities a second digital implementation was made using a set of Infineon FETs. These FETs have a higher gate resistance (1.2 ohms rather than 0.5 ohms) but are otherwise very similar in terms of important parameters such as drain-source on resistance and switching losses. In the data that follow, the digital control results using the Infineon FETs will be referred to as “Digital Infineon”.

It was found that using ZL2005 “Efficiency Optimized Driver Dead time Control” the dead time setting capabilities can be used for a quick replacement of FETs, and, which is shown in this case study, can be used for efficiency improvements.

The actual FETs used in our evaluation are summarized in the table below, and references to the FET datasheets are also contained in the references section.

	Analog	Digital Infineon	Digital Renesas
Low Side	HAT2166H	BSC029N025S	HAT2166H
High Side	HAT2168H	BSC072N025S	HAT2168H

3 Measurement Results

This section contains the results of the electrical measurements performed on the various regulator configurations. Test data for the Renesas FET digital configuration is less complete than that of the Infineon FET digital configuration due to time constraints. All measurements were taken with an input voltage of 12V and at room ambient temperature. The regulator output voltage was set to either 3.3V or 1.5V by means of the appropriate programming resistor.

3.1 Efficiency and Power Dissipation

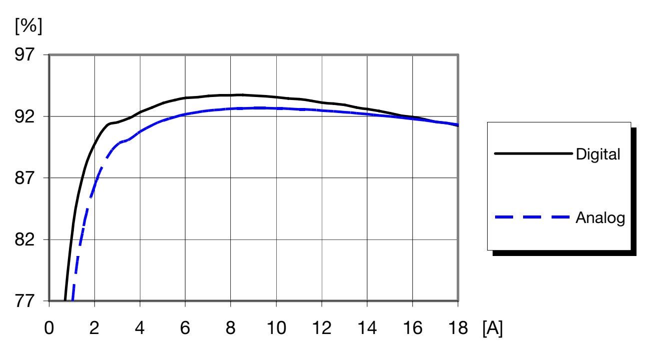

Fig. 1) Eff @ 3.3 V - Renesas Digital

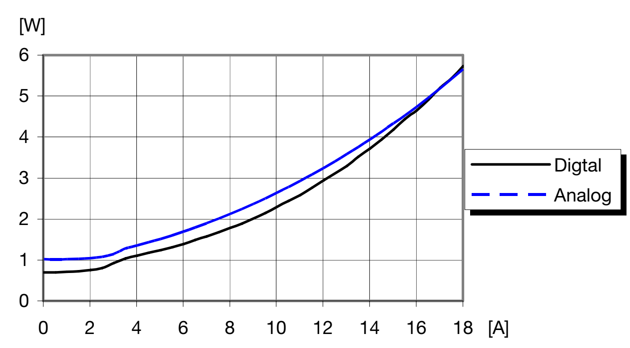

Fig. 2) Pwr Disp @ 3.3 V - Renesas Digital

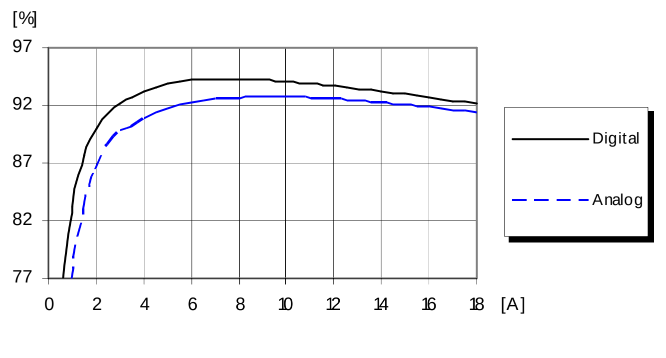

Fig. 3) Eff @ 3.3 V - Infineon Digital

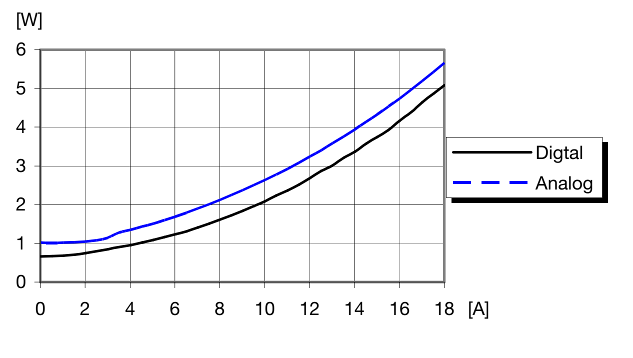

Fig. 4) Pwr Disp @ 3.3 V - Infineon Digital

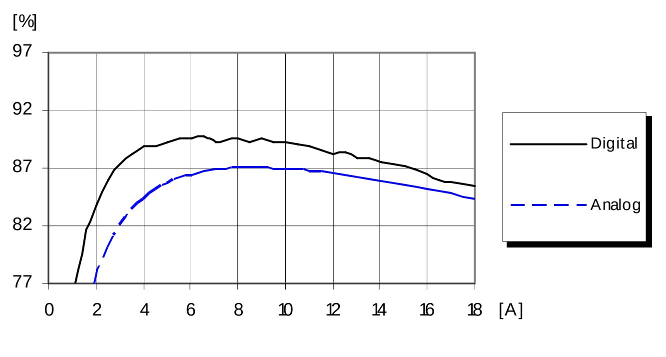

Fig. 5) Eff @ 1.5 V - Infineon Digital

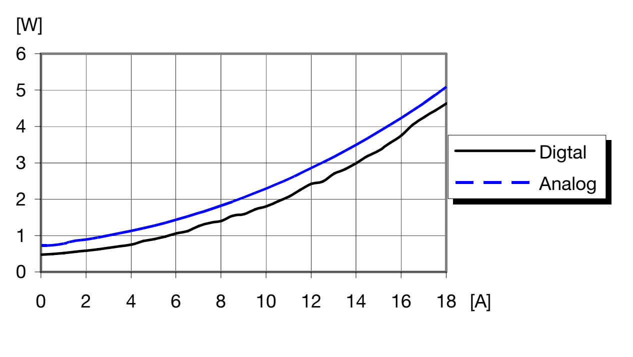

Fig. 6) Pwr Disp @ 1.5 V - Infineon Digital

Comparison of Digital Performance vs. Analog

	Digital Infineon		Digital Renesas	
	Eff	Pwr Disp	Eff	Pwr Disp
3.3V 18A	+ 0.8%	- 0.57 W	Same	Same
1.5V 18A	+1.2%	- 0.45 W	No Data	No Data

At full load, the Renesas digital configuration is equal to the analog solution, but does exhibit some improvement at lower load currents. The Infineon FET digital implementation is clearly better than the benchmark analog solution for both efficiency and power dissipation.

As can be seen from the Power dissipation diagrams in Fig 2, 4 and 6, there is a reduction in power dissipation in the digital implementation. This is due to the elimination of house-keeping and protection circuitry, which is necessary for the analog DC/DC solution.

3.2 Output Regulation

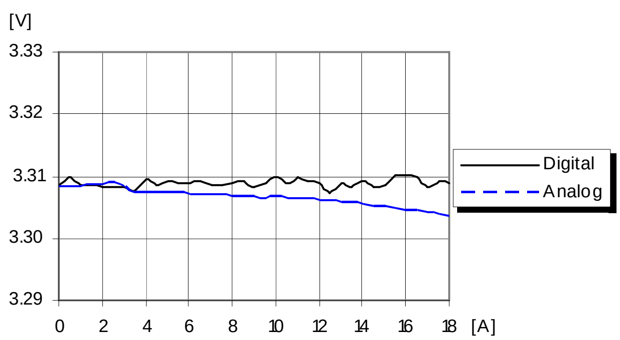

Fig. 7) Regulation @ 3.3 V – Infineon Digital

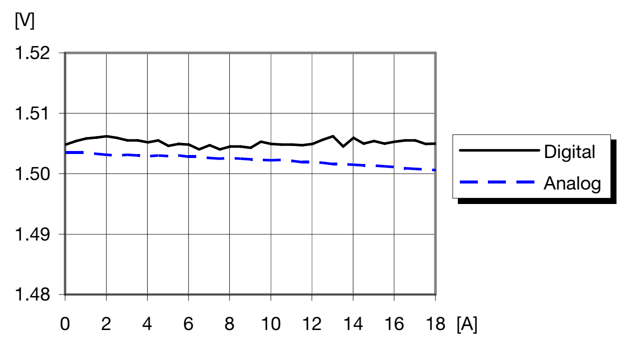

Fig. 8) Regulation @ 1.5 V - Infineon Digital

The output regulation vs. load for Infineon and Renesas Digital implementation were identical. For simplicity, only Infineon digital measurements are shown, see Fig 7 and 8. The output regulation vs. load current of the Infineon digital and the analog solution are essentially the same. The slightly better performance for the digital solution exhibited in the above figures is due to small differences in the test setup used for the measurement of the analog and digital regulator.

3.3 Dynamic Performance

Output ripple and noise and output load transient response were measured for both the analog and the Infineon Digital regulators. This testing was done at an output voltage of 3.3V. The filter used for the ripple and noise measurement consisted of a 0.1 uF ceramic and a 10 uF tantalum capacitor in parallel as defined in the datasheet for the PMH regulator. The dynamic load used for the transient response measurement consisted of a step change from 18 A to 9 A and then back to 18 A.

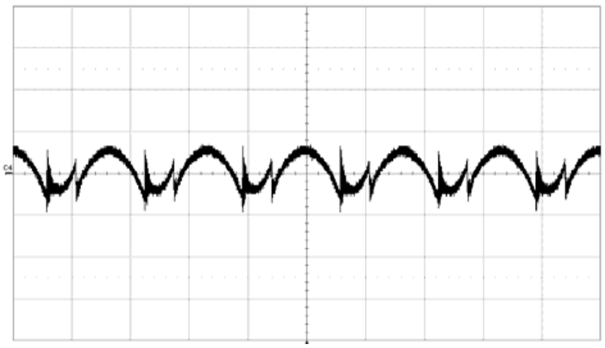

Fig. 9) Ripple & Noise – Analog (20mV/div, 2μs/div)

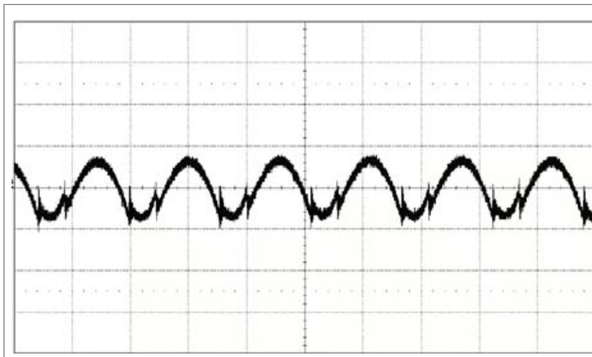

Fig. 10) Ripple & Noise - Infineon Digital (20mV/div, 2μs/div)

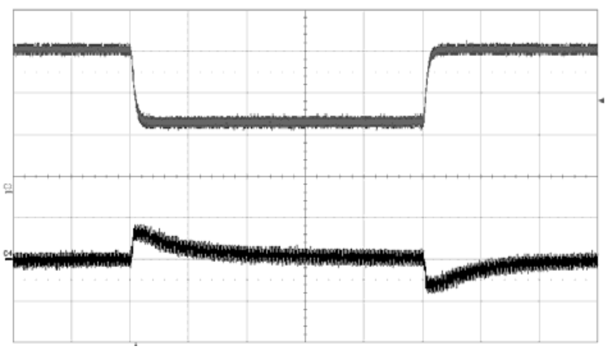

Fig. 11) Transient Response – Analog.
Top trace: Load current (10A/div).
Bottom trace: Output voltage (100mV/div).

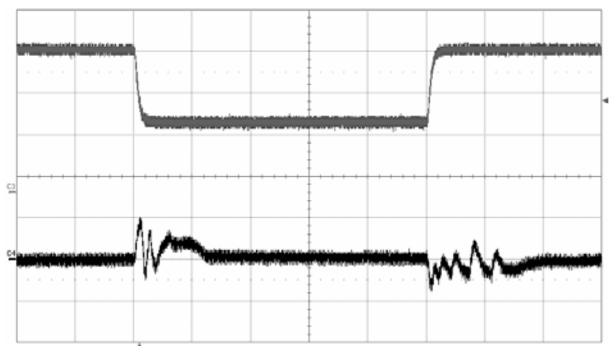

Fig. 12) Transient Response - Infineon Digital
Top trace: Load current (10A/div).
Bottom trace: Output voltage (100mV/div).

The measured ripple and noise for the digital solution is slightly higher than the analog. The main reason for this is the difference in capacitance value, due to component tolerances in the external 330μF capacitor. There is also a minor variation in-between the two due to the previously mentioned small difference in switching frequency. For practical reasons the ripple and noise may be considered the same. The analog solution provided a traditional smooth voltage response to the dynamic load current change as can be seen in Fig 11. The peak amplitude is in the range of ± 70 mV. The digital solution, which was programmed to work in Non-Linear Response mode (see section 5.11 of the referenced Zilker Labs datasheet), shows similar peak amplitude at low-to-high load transitions, and somewhat higher peak amplitude at high-to-low load transitions as can be seen in Fig 12. Due to the NLR mode operation, the peak is distributed over time generating a burst of peaks smaller than it would have been with the NLR turned off. Time did not permit optimization of the NLR settings, but we feel that the dynamic response waveform can be improved. Even as it is now, the amplitude of the voltage response is similar to that of the analog regulator response.

Our overall conclusion is that the digital approach offers similar or improved electrical performance when compared to an analog control design.

4 Calculated Results

By using the BOM of the respective analog and digital designs, estimates can be obtained for such items as packaging area, cost and reliability. The comparisons in this section are between the benchmark PMH analog regulator and the digital control regulator using the Renesas FETs. The cost estimates in this paper are general in nature due to the uncertain trends in component costing, but there is sufficient data to project relative cost differences between the two approaches.

4.1 Component Count and Packaging

The digital implementation resulted in a very significant reduction in component count relative to the benchmark analog regulator. Neglecting I/O pins (to be discussed later), the component count for the digital regulator is 21 vs. 58 for the PMH analog regulator, constituting a 64% reduction. This reduction will drive improvements in cost, packaging size and reliability.

One of the main assumptions of this particular case study is that we are only addressing the user benefit of using digital control internal to the POL regulator without any system level digital power management functions. Consequently there does not need to be any dedicated I/O pins for the purpose of digital communication between the regulator and the user's system. This is consistent with the pin design of the PMH regulator module (10 total pins). The PCB used in the digital implementation includes 3 additional pins dedicated to a digital interface between the regulator and the system (13 total pins). Since these pins were not used in this study, it was felt that the most meaningful comparison could be obtained by ignoring the pins.

Even though the PCBs of the two regulators have the same area, there is a significant difference in their packaging density due to the lower component count of the digital solution. Below are photographs of both sides of the populated analog and digital regulator PCBs.

Fig 13) Analog POL – Front Side

Fig 14) Analog POL – Back Side

Fig 15) Digital POL – Front Side

Fig 16) Digital POL – Back Side

Obviously the digital POL regulator layout is not optimized in terms of packaging and would not be used for a production unit. We estimate that a production version of the digital design could be vastly improved in either of two ways:

- The PCB board area could be reduced by 40 to 50% while maintaining the 18 A current rating, resulting in significant improvements in packaging density for the end user.
- If the PCB board area is maintained with the same dimensions as the PMH modules, the output current rating could be approximately doubled, resulting in over 35 A of output current. This of course will require changes to the power train components to accommodate the increased current levels.

We conclude that the digital approach results in very significant benefits in terms of component count and packaging density when compared to the analog design.

4.2 Cost Estimates

It is premature to do an accurate quantitative assessment of BOM costs of the two approaches since the digital design is new and Ericsson does not yet have experience with large quantity production purchases of the required components. However, our preliminary, and forward-looking, analysis convinces us that there will be definite overall cost savings associated with the digital design.

In terms of BOM cost, the 10 pin version of a digital regulator should be definitely less than the present PMH design, due to the reduction in parts count. A 13 pin version with a communication interface, while slightly more expensive, should also be less than the analog implementation. There should also be cost savings during the assembly process due to the reduction in the number of components.

Our conclusion is that the production cost (and corresponding customer price) of a digital regulator should be less than that of a unit with the same functionality using analog control once quantities increase.

4.3 Reliability Estimates

Ericsson does extensive failure rate analysis and reliability predictions for all of its products. We use the methodology described in Telecordia SR332, issue 1, black box technique. MTBF predictions are made under the conditions of full output power at an ambient operating temperature of +40 degrees C.

Using the above assumptions and methodology, the predicted reliability for the PMH analog and Zilker Labs ZL2005 digital approach are as shown below:

PMH8918L Analog	3.87 million hours
Digital	4.31 million hours

The vast reduction in component count makes the digital version more reliable even with the addition of some complex components such as memory in the digital control chip. In an 18 A digital version built on the existing PCB area such as shown in Figures 15 and 16, the lowered component density would result in lower operating temperatures for the circuitry. This would further decrease the failure rate and increase the MTBF. This effect is not included in the above calculated reliability estimates.

We conclude that a digital control approach exhibits meaningful improvements in reliability when compared with a traditional analog regulator.

5 Conclusion

This paper is a case study that compares the differences, as seen by the end user, between power regulators implemented with analog and digital control techniques. We have tried to keep the comparison as fair and “apples to apples” as possible. While focused on a single design at an output current of 18 A, we believe that it is likely that many of the conclusions may, in general, be extended to other power module families.

Based upon the electrical measurements and calculations performed during the study, we conclude the following:

- The electrical performance, including efficiency, of the digitally controlled converter is equal to or better than the analog version. Additional work needs to be done to optimize the dynamic load response of the digital design.
- The digital solution results in more than a 60% reduction in parts count. This significantly increased level of integration will reduce the materials and assembly costs of the converter.
- The reduced parts count results in a reduction in required real estate for the converter circuitry. This can be used either to reduce the size of the converter or to increase the power output within the present size envelope. In any case, the power density can be significantly increased using digital control techniques.
- The reduced parts count will increase the predicted reliability.

These user benefits are achieved without any extra effort on the part of the OEM customer. The digital regulator module may be used interchangeably with the analog version and requires no specialized interface or design accommodation.

This study was conducted in Q2 – Q3 of 2006 and to the best of our ability reflects the situation in the 2006/2007 timeframe. If history is a guide, we expect that the benefits will swing even more in favour of a digital approach in subsequent years as parts availability, design experience and component pricing for digital control designs reach a higher level of maturity.

Ericsson plans to continue to explore the design of regulators and converters using digital controls. In the near future we will build, characterize and qualify designs using larger volume pilot runs. We also plan to further optimize the control designs and power train configurations to offer the most possible benefit to our customers.

6 Glossary

BOM: Bill of Material

FET: Field Effect Transistor

I/O: Input / Output

MTBF: Mean Time Between Failure

OEM: Original Equipment Manufacturer

PCB: Printed Circuit Board

POL: Point of Load

PWM: Pulse Width Modulation

7 References

- Ericsson PMH8918L Datasheet
- Zilker Labs ZL2005 Datasheet
- Infineon BSC029N025S G FET Datasheet
- Infineon BSC072N025S G FET Datasheet
- Renesas HAT2166H FET Datasheet
- Renesas HAT2168H FET Datasheet