# 60 GHz Single-Chip Front-End MMICs and Systems for Multi-Gb/s Wireless Communication

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***Abstract*—Single-chip 60 GHz transmitter (TX) and receiver (RX) MMICs have been designed and characterized in a 0.15 $\mu$m ($f_T$ ~ 120 GHz/$f_{MAX}$ > 200 GHz) GaAs mHEMT MMIC process. This paper describes the second generation of single-chip TX and RX MMICs together with work on packaging (e.g., flip-chip) and system measurements. Compared to the first generation of the designs in a commercial pHEMT technology, the MMICs presented in this paper show the same high level of integration but occupy smaller chip area and have higher gain and output power at only half the DC power consumption. The system operates with a LO signal in the range of 7–8 GHz. This LO signal is multiplied in an integrated multiply-by-eight (X8) LO multiplier chain, resulting in an IF center frequency of 2.5 GHz.**

**Packaging and interconnects are discussed and as an alternative to wire bonding, flip-chip assembly tests are presented and discussed. System measurements are also described where bit error rate (BER) and eye diagrams are measured when the presented TX and RX MMICs transmits and receives a modulated signal. A data rate of 1.5 Gb/s with simple ASK modulation was achieved, restricted by the measurement setup rather than the TX and RX MMICs. These tests indicate that the presented MMICs are especially well suited for transmission and reception of wireless signals at data rates of several Gb/s.**

***Index Terms*—60 GHz, flip-chip, GaAs, highly integrated, image rejection, mHEMT, MMIC, multi-functional, packaging, receiver, RFIC, RX, single-chip, transmitter, TX, V-band.**

## I. Introduction

FUTURE communication networks aim at "quadruple play," i.e., providing a simultaneous service for voice, video, data, as well as mobility or nomadism, i.e., connected everywhere. This requires wireless access networks with very high capacity. High data-rate wireless access requires broad frequency bands, and a sufficiently broadband spectrum can be obtained in the millimeter-wave (mm-wave) bands. The mm-wave band has several advantages: large spectral capacity, small antennas, and compact and light equipment. In the 60 GHz band, where the oxygen absorption has its maximum (10–15 dB/km), there is also the additional benefit of reduced co-channel interference. Therefore, this mm-wave band enables dense (< 1 km) wireless communication, due to shorter cell re-use distance, as well as access to worldwide allocated non-regulatory frequency bands [1]–[3].

Today, several companies provide 60 GHz data links for Gigabit Ethernet (1.25 Gb/s) bridges between LAN networks. It is expected that the use of 60 GHz technologies will extend to other areas, such as fixed wireless access networks [3]. Inter-vehicle and roadside communications in Intelligent Transport System (ITS) applications, as well as the quasi-cellular Mobile Broadband Systems (MBS) [4], are other areas where 60 GHz technologies will be implemented in the future. However, the 60 GHz band is not limited only to communication systems, the mm-wave market has traditionally been focused to military and space applications, i.e., radar and sensing systems, and the 60 GHz band is very well suited also for those applications.

During the last few years, a number of publications describing MMIC chip-sets suitable for broadband mm-wave applications have been published [5]–[19]. For all the applications mentioned above, it is important to reduce the number of interconnects and the cost of the chip itself. A high integration level is therefore necessary and a single MMIC chip should contain as much as possible of the mm-wave front-end.

Recently, our group at Chalmers University of Technology has presented highly integrated 60 GHz transmitter (TX) and receiver (RX) chips using a commercial foundry process based on a 0.15 $\mu$m gate length GaAs pHEMT technology[1] [20]. This paper is a continuation of the work presented in [21] and reports on the development of the second generation of 60 GHz TX and RX chips using a foundry process based on a 0.15 $\mu$m gate length GaAs mHEMT technology.[2] Together with [12] and [20], these chips show the highest level of integration yet presented in the 60 GHz band.

Packaging and interconnects are also important issues when integrating the MMIC chips into a complete transceiver module. As an alternative to wire bonding, flip-chip assembly tests have been evaluated and are also presented and discussed.

The small size (a few mm$^2$) of an antenna at these frequencies opens up the possibility of incorporating the antennas into the

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[1]WIN pp15-20 0.15 $\mu$m pHEMT—www.winfoundry.com

[2]WIN mp15-01 0.15 $\mu$m mHEMT—www.winfoundry.com

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package. Using standard thin-film technology, it is possible to integrate planar antennas with an MMIC chip-set performing transmit and receive functions in a 60 GHz module, which has also been done in our group and is presented in [22].

The paper is outlined as follows: Section II presents a comparison between GaAs HEMT and silicon technologies. Section III describes the MMIC technology used. Section IV is an overview of the TX and RX chips. Section V presents the local signal generation chain, up and down converting mixers and the three-stage amplifier used as both post amplifier (PA) in the TX and low noise amplifier (LNA) in the RX MMIC. Sections VI and VII presents the measured results of the TX and RX chips, respectively. Packaging and interconnect issues including flip-chip assembly are presented and discussed in Section VIII. Thereafter, system level measurements with the TX and RX chips interconnected are presented in Section IX. Section X compares with the work of others and discussion and summary are found in Section XI and finally, Section XII concludes the paper.

## II. GaAs HEMT Versus Silicon Technologies

Traditionally, compound semiconductors have possessed the best overall performance for mm-wave MMICs and GaAs based pHEMT technologies have in particular been the true work horse for MMICs operating in the mm-wave range. In the early 1990s, the mHEMT was developed [23] and is now in the phase of commercialization at several III-V foundries around the world. By using a graded buffer beneath the channel, the indium concentration in the channel of the mHEMT device can be allowed to increase compared to the pHEMT device. This result in devices with improved $f_{\mathrm{T}}$, $f_{\mathrm{MAX}}$, noise, and overall DC performance.

However, silicon technologies are emerging strongly and several mm-wave MMICs and RFICs[3] have been designed and presented during the last couple of years [12]–[19]. Those MMICs will be summarized and compared with the presented GaAs mHEMT chipset in Section X of this paper. Both SiGe-based HBTs and CMOS silicon technologies have been used where the latter is often highlighted as the most interesting due to its low cost and the former due to better, close to III-V-s, high-frequency performance. Furthermore, a combination of HBTs and CMOS can be found in the increasingly popular BiCMOS processes. Another promising technology for the future is silicon-on-insulator (SOI) CMOS processes which are a very interesting technology for future mm-wave MMIC design. In an SOI process, a thin silicon device film on an insulating layer yields a process with improved isolation and noise performance. A common problem for all silicon technologies is the lossy substrate which results in worse performance for the passive circuitry compared to III-V compound semiconductors. This is the reason why silicon based MMICs often uses active devices to replace passive circuitry, e.g., active instead of passive baluns. The problem with the lossy passive circuitry has led to the development of certain RF-CMOS processes. Those are often based on a standard digital process with one modified metal layer or one or more post processed layer of thick metals on a low loss dielectric which facilities the design of relative low loss high frequency passive components. Furthermore, the RF-CMOS processes incorporates elements which are not at all available in a standard CMOS process such as thin-film resistors and MIM capacitors, essential components in almost any analog design, regardless of the frequency of operation. But maybe the most critical difference between a RF-CMOS and a standard CMOS process is the availability of high-frequency models of both passive and active devices in the designkit of the former.

The two main driving forces for the development of the silicon technologies towards mm-wave MMICs are the lower cost compared to compound semiconductors and the possibility of integrating both digital and analog designs on the same chip. The lower cost is not only due to lower production costs which origins from the cheaper material but also from the large number of silicon foundries which offers mature and stable processing together with high yield and large wafer sizes. Although the vast majority of this processing is done in processes not suitable for mm-wave MMIC design, the mm-wave MMIC community anyway benefits from the widespread know-how in the industry regarding silicon processing. Furthermore, the fact that a CMOS chip may include both analog front-end parts and some (or in the future, all) digital electronics to make up a true single-chip mm-wave transceiver which drastically would reduce the cost for the overall system in a high-volume product.

Although a majority of mm-wave MMICs designers and researchers seem to agree that silicon is the cheapest technology available, this is an exaggerated simplification. The total cost for an mm-wave system is made up of several parts and the overall lowest cost for every individual system differs. Important system parameters are level of integration, partitioning between hardware and software, volume, design time, cost of hardware and software, etc. On this level, silicon technologies have the already mentioned obvious advantage of possible integration of both analog and digital parts on the same chip. On chip level, the total cost is once again made up by several parts such as design time, photo mask fabrication, wafer manufacturing, and testing. Of those parts, design time and photo mask fabrication is not dependent of the production volume while wafer manufacturing and testing scales with volume. Design time and testing of the different technologies can be assumed to be roughly equal. Thus, in order to compare different MMIC technologies, it is absolutely crucial to determine the expected production volume. For GaAs pHEMT and mHEMT technologies, the photo mask fabrication is orders of magnitudes cheaper compared to a CMOS processes with similar high frequency performance. SiGe-based HBTs are even more expensive on this point. The main reason for this difference in mask cost is the number of masks required, GaAs HEMT technologies uses typically only one third or one fourth of the number of masks required when processing silicon. Regarding the wafer manufacturing cost, the situation is the opposite, the GaAs HEMT technologies are now in the order of magnitudes more expensive compared to its silicon counterparts. In particular, it can be noted that the cost for the GaAs epi wafer may approach 50 % (!) of the total finished wafer manufacturing cost. There are also other issues which makes silicon

[3]Throughout this paper, RFICs will often be refered to as MMICs since the difference between these two groups many times are marginal in the mm-wave range.

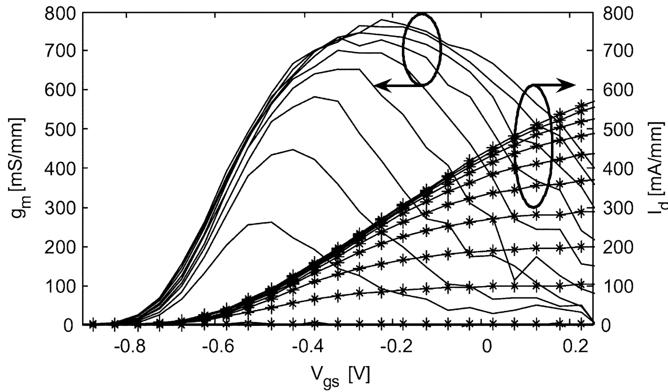


Fig. 1. Measured $g_m$ and $I_D$ for a 2 × 50 $\mu$m mHEMT device at different $V_{DS}$.

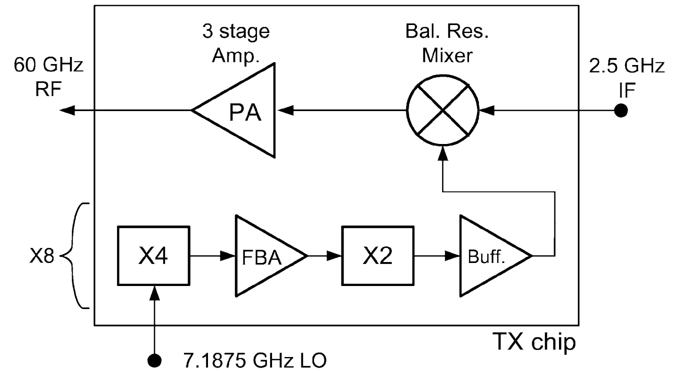


Fig. 2. TX chip circuit block diagram.

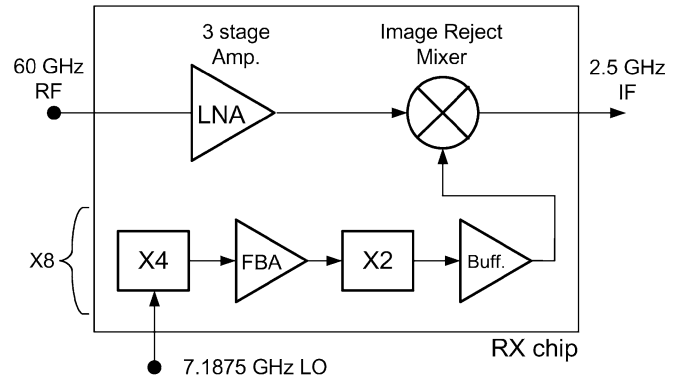


Fig. 3. RX chip circuit block diagram.

processing more suited for large scale production. Considering the large silicon foundries, those issues include for example machine throughputs and the possibility to pool spare parts and maintenance over a large equipment base. Furthermore, many of the machines in such a foundry can be re-used for different silicon technologies and hence make it possible for a more efficient use of the machine park. Those are benefits which a much smaller GaAs foundry does not have [24].

Thus, the simple rule of thumb is that silicon, and particularly CMOS, is indeed the cheapest technology available for mm-wave MMICs *but only for very large volumes*. Those mass market products include circuits for WLAN, WPAN, and similar applications which come in multi-million series and the cost of the used chip set are of uppermost importance. On the other side of the scale are low volume production such as space instruments, radiometers, certain radar systems, and radio link products. For already discussed reasons, it is difficult to draw an exact line when GaAs HEMT or silicon technologies are advantageously from a cost point of view, but with the current available commercial technologies, this limit is in the order of several hundred thousands of manufactured MMICs. Furthermore, with the ongoing development of the silicon technologies which results in better high frequency performance for a lower cost, the break-even limit of manufactured MMICs will decrease in the future. However, it is the authors' strong belief that the GaAs HEMT technologies will have a cost advantage over its silicon counterparts in many products in the foreseeable future. Furthermore, if the noise, power handling capability, and high quality passive circuitry are considered, it can be concluded that GaAs HEMT technologies will continue to play an important role for low-volume mm-wave MMICs in the future. The presented mHEMT MMICs are intended for that low-volume market and can be used for such a broad spectrum of applications from high data rate communications to radiometer or radar applications due to their multipurpose topology and broadband characteristics.

## III. MMIC Technology

In this work, an mHEMT MMIC process from WIN Semiconductors in Taiwan was used[2]. The device structures are grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. For device fabrication, E-beam lithography is used to define the 0.15 $\mu$m gate; Au/Ge/Ni/Au metals are evaporated and alloyed with a rapid thermal processing (RTP) system providing a low contact resistance around 0.15 $\Omega$·mm. Concerning high frequency characteristics, the devices show a cut-off frequency $(f_T)$ of 120 GHz and a maximum oscillation frequency $(f_{MAX})$ exceeding 200 GHz. Regarding passive components, TaN resistors with a sheet resistance of $50 \pm 1\Omega$/square were fabricated together with MIM capacitors with a capacitance of $400 \pm 40$ pF/mm$^2$. Measured transconductance $(g_m)$ and drain current $(I_D)$ characteristics at different $V_{DS}$ (0.05 V step) versus $V_{GS}$ are found in Fig. 1 for a 2 × 50 $\mu$m mHEMT device. Maximum $I_D$ density is 730 mA/mm and the breakdown voltage is as high as 10 V.

The first generation of 60 GHz single-chip TX and RX MMICs developed in our group at Chalmers University of Technology [20] used a 0.15 $\mu$m gate length pHEMT technology[1] from the same foundry as provided the mHEMT technology. The passive components in the pHEMT technology are identical to the ones used in the mHEMT counterpart. However, the pHEMT devices showed a $f_T$ of $88 \pm 2.2$ GHz and an $f_{MAX}$ of $183 \pm 11.2$ GHz for volume production wafers. Concerning DC characteristics, maximum $g_m$ and $I_D$ were measured to 490 mS/mm and 660 mA/mm, respectively. The pinch-off voltage was found to be $-1.1$ V which is 400 mV lower, i.e., more negative, compared to its mHEMT counterpart.

In circuits like resistive mixers where the HEMT device operates as a gate-voltage controlled resistor with zero drain bias,

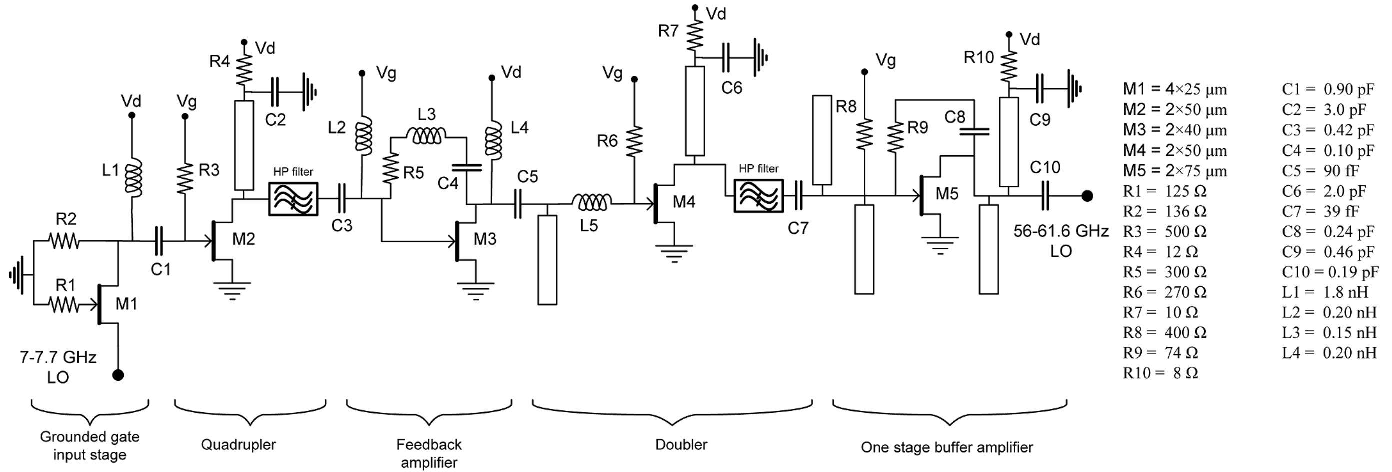


Fig. 4. Schematic of the multiply-by-eight (X8) LO multiplier chain.

$r_{DS}$ versus $V_{GS}$ is an important parameter. For maximum conversion efficiency in such circuits, the HEMT would ideally switch between infinite off-and zero on-resistance. Particularly, the on-resistance needs to be low since the off-resistance in practical circuits is high enough for efficient switching. The on-resistances for the mHEMT/pHEMT devices are 1.2/1.5 $\Omega$·mm, respectively.

## IV. TX and RX Chip Overview

The TX chip consists of an X8 LO multiplier chain, a balanced resistive mixer and a three-stage amplifier as will be described later in this paper. The X8 LO multiplier chain is a multifunctional design of its own consisting of a quadrupler (X4), a feed back amplifier (FBA), a doubler (X2) and a buffer amplifier (Buff). The block diagram is shown in Fig. 2. The balanced resistive mixer produces two sidebands and it is assumed that the unwanted sideband is removed (if necessary) by filtering in an external filter located after the three-stage amplifier in the TX chip.

The RX chip is designed in a similar way as the transmitter chip and consists of an X8 LO multiplier chain, an image reject mixer and a three-stage amplifier. The block diagram is shown in Fig. 3.

## V. Sub-Blocks in the TX and RX Chips

### A. Local Signal Generation

A common approach to obtain a high purity local oscillator (LO) signal with low phase noise in the mm-wave range is to multiply a low frequency LO signal up to the wanted frequency. This has two advantages; one is that the VCO could be directly locked to a phase locked loop (PLL), typically available up to 15 GHz, without the need of power consuming frequency dividers. The other advantage is low phase noise levels. Fundamental frequency oscillators at V-band are possible to design but their phase noise performance will typically be worse compared to a complete design using a good quality low frequency LO signal together with a multiplier chain, multiplying the low frequency signal to the desired V-band LO signal. The added phase noise by the multiplication itself is theoretically $20 \times log(N)$ where $N$ is the multiplication order [25]. For the multiply-by-eight (X8) LO multiplier chain used in this work, the phase noise added by the multiplication itself becomes 18.06 dB.

The local signal generation on-chip is implemented as an X8 LO multiplier chain which multiplies an input signal in the 7–8 GHz range to the wanted LO frequency in the vicinity of 60 GHz. Although not used in the presented TX and RX MMICs, an mHEMT voltage controlled oscillator (VCO) suitable for integration in a possible future next generation of the TX and RX MMICs was also designed and is presented in [26]. The X8 is a multifunctional design of its own consisting of a quadrupler (X4), a feed back amplifier (FBA), a doubler (X2) and a buffer amplifier. Schematic of the X8 is shown in Fig. 4.

An output power of more than 6 dBm is obtained between 53 and 60 GHz with a maximum efficiency of 6% at 55 GHz. The efficiency is calculated as the power of the wanted output frequency divided by the total power added to the circuit. The phase noise degradation is measured as the added phase noise by the X8 in addition to the theoretical 18.06 dB inherently added by the multiplication. The measured phase noise degradation ($< 1$ dB), spectral purity ($> 18$ dB of suppression of all other harmonics), efficiency, and power consumption indicates that the mHEMT X8 multiplier circuit is a successful design for LO multiplier chain application in the single-chip TX and RX MMICs. Theory of active multipliers in general together with a detailed description of the design of the X8 LO multiplier chain and its performance can be found in [27].

### B. Balanced Resistive Mixer

In the TX chip, a balanced resistive mixer (BRM) is used. A balanced mixer topology is chosen since it offers high LO to RF isolation over a large bandwidth compared to other mixer topologies. A schematic of the BRM is found in Fig. 5.

The IF is transformed from unbalanced to balanced signal in a broadband second-order lattice balun (SOLB) [28] and applied to the sources of the HEMTs through two low-pass filters.

The BRM shows broadband IF performance with a 3 dB bandwidth of 1.2 GHz (2.2–3.4 GHz) with 11.8 dB of conversion loss ($L_C$) at 2.5 GHz. The shape of the $L_C$ versus IF

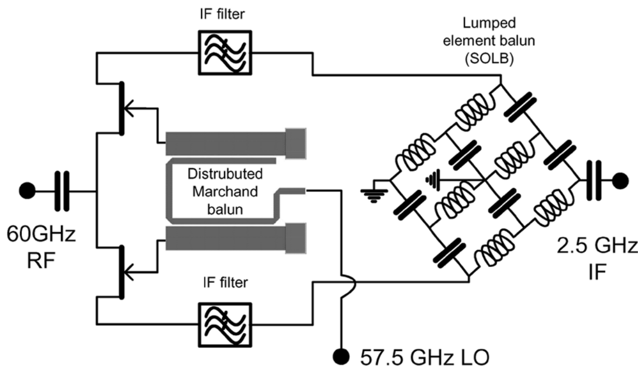


Fig. 5. Schematic of the balanced resistive mixer (BRM).

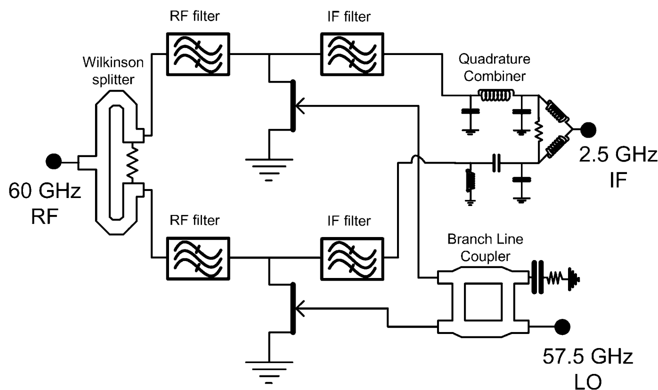


Fig. 6. Schematic of the image reject mixer (IRM).

frequency characteristic is mainly determined by the insertion loss and balance of the SOLB. Furthermore, since the BRM is used in the TX MMIC, an important parameter is the LO to RF isolation since any residual LO signal at the RF port will be amplified by the three-stage amplifier and transmitted together with the wanted RF signal. The LO to RF isolation was measured to be more than 28 dB in the frequency band of interest.

## C. Image Reject Mixer

In this work, the image suppression is performed in an image reject mixer (IRM). To minimize the overall power consumed by the system in which the RX chip will be used, the combination of the two 90° out of phase IF signals are performed on-chip in an ultra broadband lumped element hybrid [29]. This allows the system to use only one, instead of two very power-consuming analog-to-digital converters which thereby significantly reduces the power consumption for the overall system.[4]

The IRM consists of two single resistive mHEMT mixers, two RF filters, two IF filters, a Wilkinson power splitter, a branch line coupler, and an IF quadrature power combiner used as IF hybrid, Fig. 6.

A breakout of the IRM was characterized as a down converter from 53 to 70 GHz with respect to conversion loss ($L_C$) and image rejection ratio (IRR). The measured 1 dB RF bandwidth was 10 GHz between 55 and 65 GHz with an $L_C$ of 11.7 dB and an IRR of 26 dB at the 60 GHz center frequency. The maximum

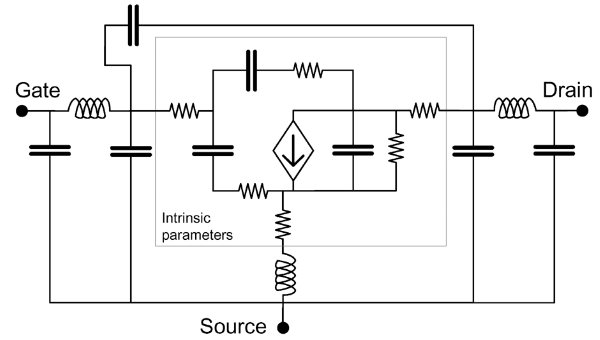


Fig. 7. Small-signal model topology.

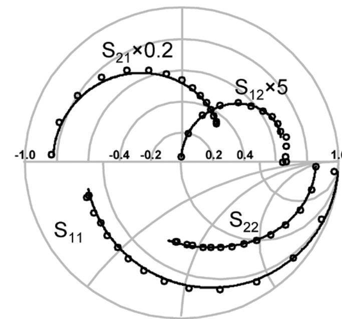


Fig. 8. Measured (circles) and simulated (solid line) S-parameters for the developed small-signal model, 1–67 GHz.

data rate that can be handled in a system is proportional to the receivers, and therefore also the mixers, IF bandwidth. The IRM shows excellent broadband IF performance with a 1 dB bandwidth as high as 1.9 GHz, between 1.1 and 3.0 GHz and an IRR better than 20 dB over a 1.6 GHz IF bandwidth, extending from 1.7 to 3.3 GHz.

## D. Broadband Small-Signal Amplifiers

The most common and well-established techniques to achieve amplifiers with very broadband response are to use either reactively matched, traveling wave distributed (TWD), or feedback amplifiers [30]. The reactively matched amplifier is well suited for broadband amplifiers with a bandwidth of one or two octaves and typically offers the lowest noise figure of the three different topologies. However, combining the low noise figure with good input matching can be troublesome. For that reason, a source inductance on the transistor is normally used in the input stage. The TWD amplifier topology accommodates two lossy transmission lines in conjugation with active devices connected in parallel to achieve ultra broadband properties. Unfortunately, a TWD amplifier is known for consuming much power and possesses a moderate gain together with a relatively poor noise figure. The feedback amplifier utilizing resistive parallel feedback can be designed to have a bandwidth of a decade or more which is lower compared to the reactively matched and the TWD amplifier topologies. Furthermore, the noise figure of the feedback amplifier is typically higher compared to the lossy matched amplifier but lower compared to the TWD amplifier. However, the feedback amplifier topology possesses several advantages compared to the other two since it is inherently stable, has good input and output matching, and a very flat gain. Another advantage is that multiple feedback stages easily can be

[4]for example: Maxim MAX108—www.maxim-ic.com

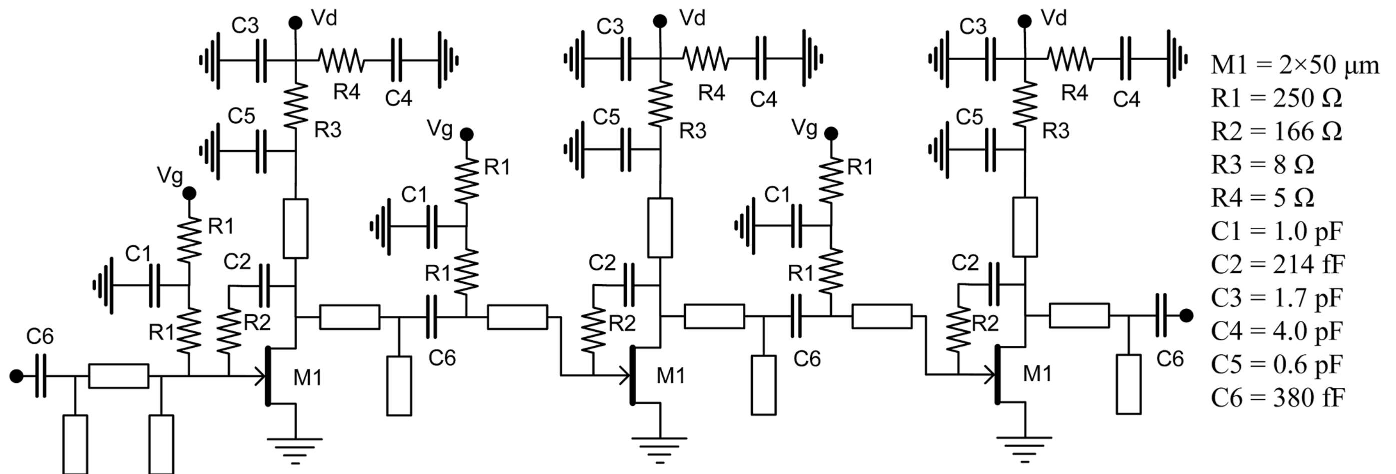


Fig. 9. Schematic diagram of the three-stage amplifier.

cascaded for higher gain. The feedback amplifier topology was therefore chosen for usage in both the TX and RX MMIC.

*1) Small-Signal Modeling:* Previous tape outs showed that the large signal EEHEMT model provided by the foundry was not accurate enough to predict the performance of broadband V-band small-signal amplifiers. A small-signal model was therefore developed based on S-parameter measurements of several different sizes of the mHEMTs. The goal was to get a small-signal model scalable by the gate width of the mHEMT device. A standard small-signal model topology was chosen according to Fig. 7 and the model parameters were extracted according to [31].

In order to make the model scalable, the intrinsic capacitances and the current gain $(\mathrm{g_m})$ were set proportional to the gate width while the internal resistances were defined as reverse proportional to the same width. External parasitics were supposed to be constant.

Test devices of the mHEMTs were measured at normal operation points but also below pinch off and strongly forward biased with zero drain voltage. The external parasitics were extracted from the measurements performed with zero drain voltage while the intrinsic parameters were extracted from the normal bias measurements. Multiple measurements on different device sizes were performed and the model parameters were calculated as the medium values after being normalized to the same device size. Finally, the exact model parameters were found by curve fitting between simulations and measurements and the whole cycle was repeated until an acceptable result was obtained. Fig. 8 shows the final fit of the measured S-parameters versus the developed small-signal model between 1.0 and 67 GHz for a $2 \times 30$ $\mu$m mHEMT with grounded source. $\mathrm{S_{21}}$ and $\mathrm{S_{12}}$ are scaled by a factor five for enhanced visibility.

*2) Three-Stage Amplifier:* A general purpose broadband three-stage amplifier utilizing resistive parallel feedback was used in both the TX and RX MMIC. Fig. 9 shows a simplified schematic. Each amplifier stage consists of $2 \times 50$ $\mu$m mHEMT device, a feedback network, and stubs for input and output matching. The gate-drain parallel feedback stabilization network consists of an *RC* network with $\mathrm{R_{FB}} = 166\ \Omega$ and

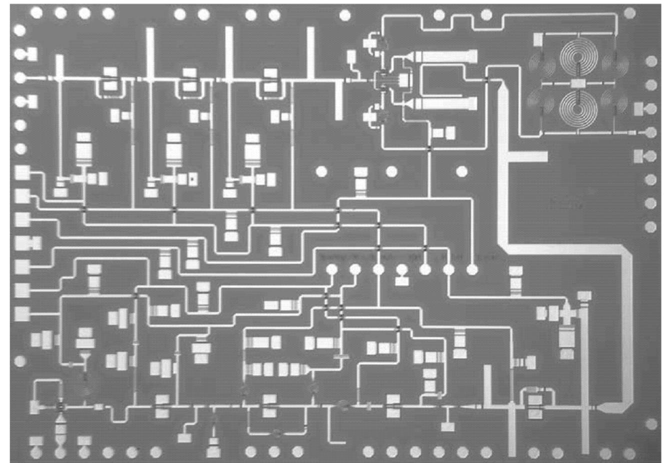

Fig. 10. The transmitter chip. The DC bias network is placed in the middle of the chip. Additional pads, for flip-chip assembly, are added along the periphery of the chip. The chip measures $4.0 \times 3.0$ mm$^2$.

$\mathrm{C_{FB}} = 214$ fF. Those values are chosen according to [32]. The gain of every feedback cell can be further peaked close to the cutoff frequency by an additional inductive series element at the output of the transistor. The layout of the feedback network is sensitive to the feedback for higher frequencies, which can be used in order to achieve a slightly positive gain slope.

The three-stage amplifier possesses more than 20 dB of gain between 20 and 67 GHz while the reflection coefficients in the same frequency range are below $-5$ and $-10$ dB for the input and output, respectively. The noise figure was measured to 6.5 dB. Furthermore, the maximum output power and the output referred 1 dB compression point were measured to 11 and 4 dBm, respectively.

## VI. TX Chip

The transmitter (TX) chip consists of the X8, the BRM, and the three-stage amplifier as described previously in this paper. A photo of the circuit is presented in Fig. 10. The chip measures $4.0 \times 3.0$ mm$^2$.

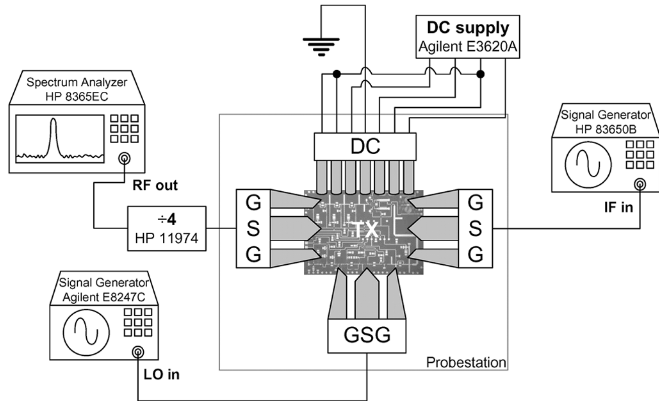


Fig. 11. Measurement setup for conversion gain, output power, RF and IF bandwidths, LO saturation, and 1 dB compression point.

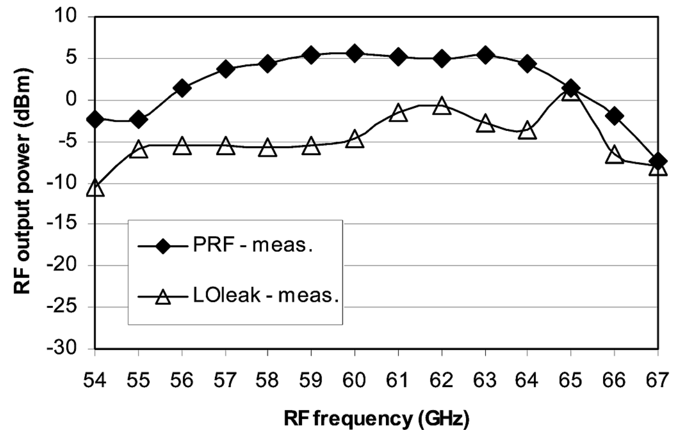


Fig. 12. Maximum output power and LO leakage power versus RF frequency for the TX chip, $f_{\rm IF} = 2.5$ GHz.

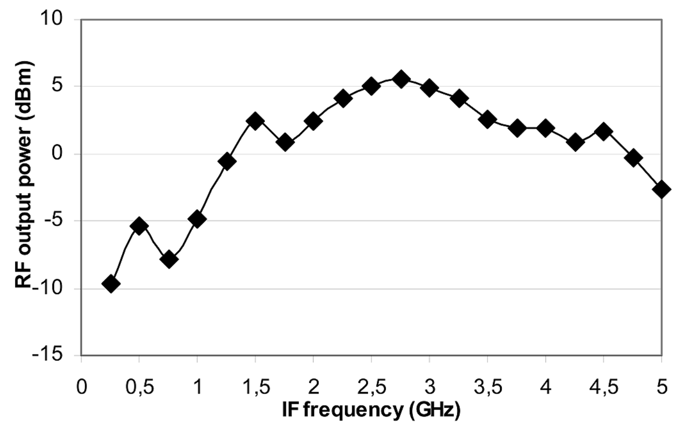


Fig. 13. Maximum output power versus IF frequency for the TX chip, $f_{\rm LO} = 7.1875$ GHz $\times 8 = 57.5$ GHz.

The bias network from the X8 is reused while the biasing of the three-stage amplifier and the mixer is incorporated. The biasing scheme is as follows; the two drain biases of the quadrupler are connected together with the drain bias of the FBA while the buffer amplifier and the three-stage amplifier both have individually biased drains. For gate bias, the quadrupler share bias pad with the doubler while the FBA, the buffer amplifier, and the three-stage amplifier are connected together to the same gate bias pad while the mixer has a gate bias pad of its own.

The pads are octagonal to be prepared for flip-chip assembly and the bias pads are centered on the chip. However, to not lose the possibility of wire bonding the chip, the bias network is also connected to (square) pads along the periphery.

The TX chip was characterized by probed measurements of conversion gain $(\mathrm{G_C})$, output power, RF and IF bandwidths, 1 dB compression point, and LO saturation with the measurement setup found in Fig. 11. Two signal generators were used as IF source (HP 83650B) and LO source (Agilent E8247C), respectively. At the RF port, a spectrum analyzer (HP 8565EC) with pre-selector (HP 11974) was used to enable measurements in the range of 50 to 75 GHz. The power settings of the signal generators were calibrated with a power meter (HP E4419B). During the measurements the nominal settings were: LO power 0 dBm; IF power 5 dBm; IF frequency 2.5 GHz, and RF frequency 60 GHz. To obtain 60 GHz RF frequency an LO frequency of 7.1875 GHz (= 57.5 GHz/8) was injected. During the measurements, the drain biases were unified. Thus, only four levels (one $\mathrm{V}_G$ bias each for the amplifiers, the mixer and the multipliers and one $\mathrm{V}_D$ bias for all the amplifiers and the multipliers) were used and adjusted to find the highest output power at 60 GHz. These optimized DC voltages results in a total DC power consumption of 420 mW.

In Fig. 12, measured maximum output power and LO (= RF-IF) leakage power related to the RF frequency band are shown. The measured 3 dB bandwidth ranges from 56.5 to 64.5 GHz with the maximum measured output power of 5.6 dBm at 60 GHz. The measured output power is about 5 dB lower compared to simulations. The difference is mainly due to the three-stage amplifier and the BRM which both have about 2–3 dB higher loss when measured compared to simulations.

The measured maximum output power versus IF frequency is found in Fig. 13. The 3 dB bandwidth is 1.5 GHz and ranges from 2.0 to 3.5 GHz with the peak output power at 2.75 GHz. The shape of the curve corresponds very well to the measured $\mathrm{L_C}$ versus IF for the BRM alone.

The measured main characteristics of the TX chip are summarized in Table III in Section XI.

## VII. RX CHIP

The receiver (RX) chip is designed in a similar way as the TX chip and consists of the X8 LO-chain, the IRM, and the three-stage amplifier as described previously. A photo of the circuit is presented in Fig. 14. The chip measures $5.5 \times 4.0$ mm$^2$.

The bias network used in the RX chip is similar to the one used in the TX chip. A seven-finger DC probe is used to apply the DC to the octagonal DC pads placed in the middle of the chip. Additional DC pads along the periphery are added to make it possible to wire bond the chip. Only three DC voltages are needed and these were adjusted to find the highest conversion gain $(\mathrm{G_C})$ at 60 GHz. These optimized DC voltages results in a total DC power consumption of 450 mW for the RX chip.

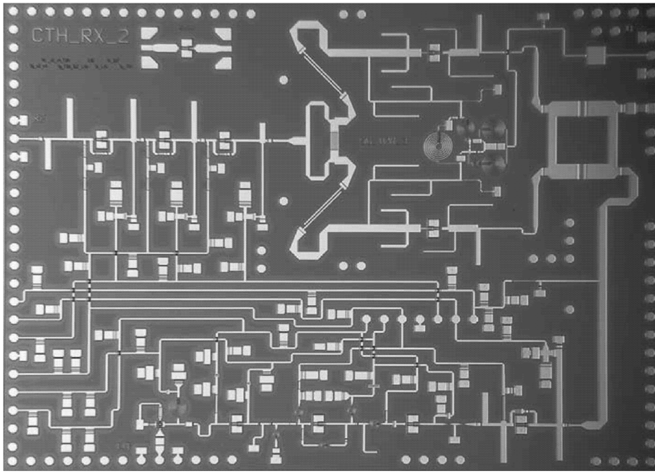


Fig. 14. The receiver chip. The DC bias network is placed in the middle of the chip. Additional pads, for flip-chip assembly, are added along the periphery of the chip. The RX chip measures 5.5 × 4.0 mm$^2$.

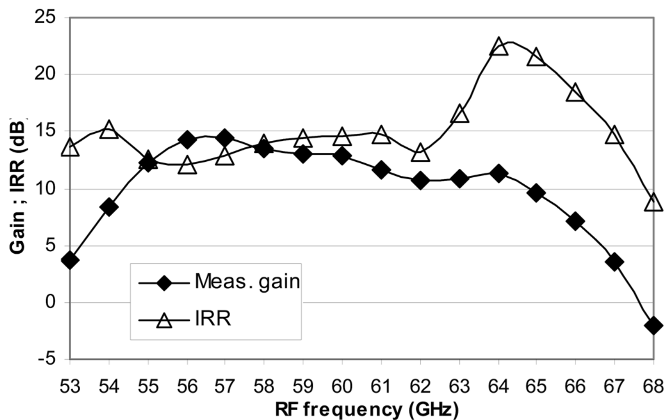


Fig. 15. Conversion gain and image rejection ratio for the RX chip versus RF frequency, $f_{\rm IF} = 2.5$ GHz.

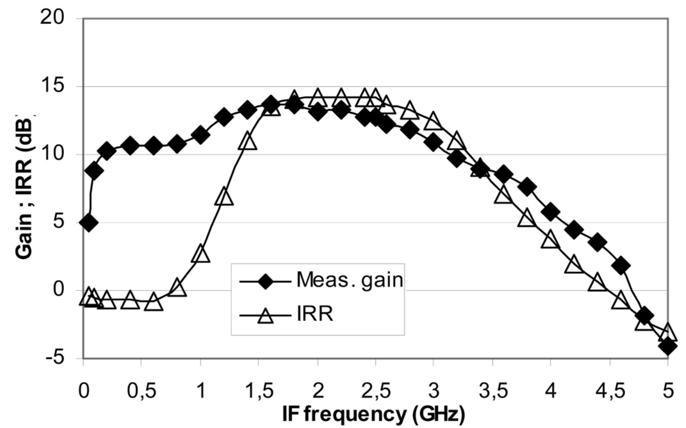


Fig. 16. Conversion gain and image rejection ratio versus IF frequency for the RX chip, $f_{\rm LO} = 7.1875 \times 8 = 57.5$ GHz.

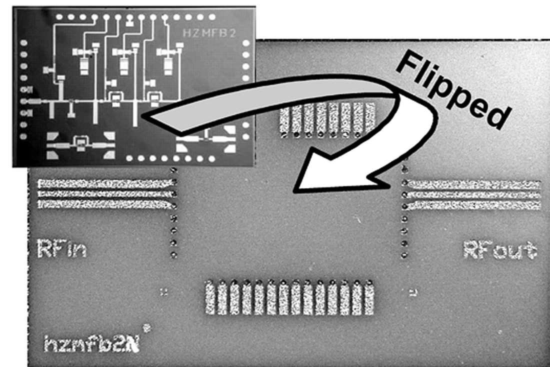


Fig. 17. Three-stage 30 to 60 GHz MMIC amplifier and the alumina thin film carrier design.

The RX chip was measured in a similar setup as the TX chip, Fig. 11, but the IF source (HP 83650B) was now connected together with an mm-wave source module (HP 83557A) to provide the V-band RF input signal. The nominal values for RF, LO, and IF frequencies were 60 GHz, 57.5 GHz ($=7.1875$ GHz $\times 8$), and 2.5 GHz, respectively. Nominal RF and LO powers were $-24$ dBm and $-1$ dBm, respectively.

The measured $\rm G_C$ and IRR for the RX chip versus RF frequency are plotted in Fig. 15. The RX chip possesses a 3 dB RF bandwidth of 10 GHz between 54.5 and 64.5 GHz with an $\rm G_C$ of 12.9 dB at 60 GHz. The IRR is above 13 dB between 57.5 and 67.5 GHz.

In Fig. 16, the measured $\rm G_C$ and IRR are plotted versus IF frequency. The 3 dB IF bandwidth ranges from 0.2 to 3.2 GHz and the IRR is above 13 dB between 1.5 and 2.9 GHz.

The measured $\rm G_C$ depends on LO power in essentially the same way for both the TX and RX MMICs. An LO power as low as $-4$ dBm is sufficient to obtain a $\rm G_C$ of more than 12 dB. Furthermore, linearity of the RX chip is characterized by the 1-dB compression point $(\rm CP_{1dB})$ and the input referred third-order intercept point (IIP3). The former was measured to $-17$ dBm at 60 GHz and the latter was measured in a two-tone test at the same frequency. Two tones separated by 100 MHz, 59.95 and 60.05 GHz, were applied on the RF port and the first and third order IF tones at 2.55 and 2.65 GHz were measured. The fundamental IF output power was plotted together with an extrapolated line with unity slope, while the third-order tone was extrapolated along a line with a slope of three. The intersection of the lines gives an input referred IP3 of $-10$ dBm for the RX chip.

Finally, the noise figure (NF) of the RX chip has been measured to 7.2 dB at 60 GHz in a measurement setup with an Agilent noise figure analyzer (NFA) N8975A. The NFA was first calibrated using an HP346A noise source connected directly to the input of the NFA. A V-band noise source (Noise Com NC5115) was then connected to the input of the RX chip and the NF was measured.

The measured main characteristics of the RX chip are summarized in Table IV in Section XI.

## VIII. Packaging and Interconnects

Packaging and interconnects are important issues when integrating MMICs into modules. The substrate that carries the MMIC chips is typically fabricated using either the more conventional material alumina $(\rm Al_2O_3)$ or a multi-layer technology such as low-temperature co-fired ceramic (LTCC) [33], high-

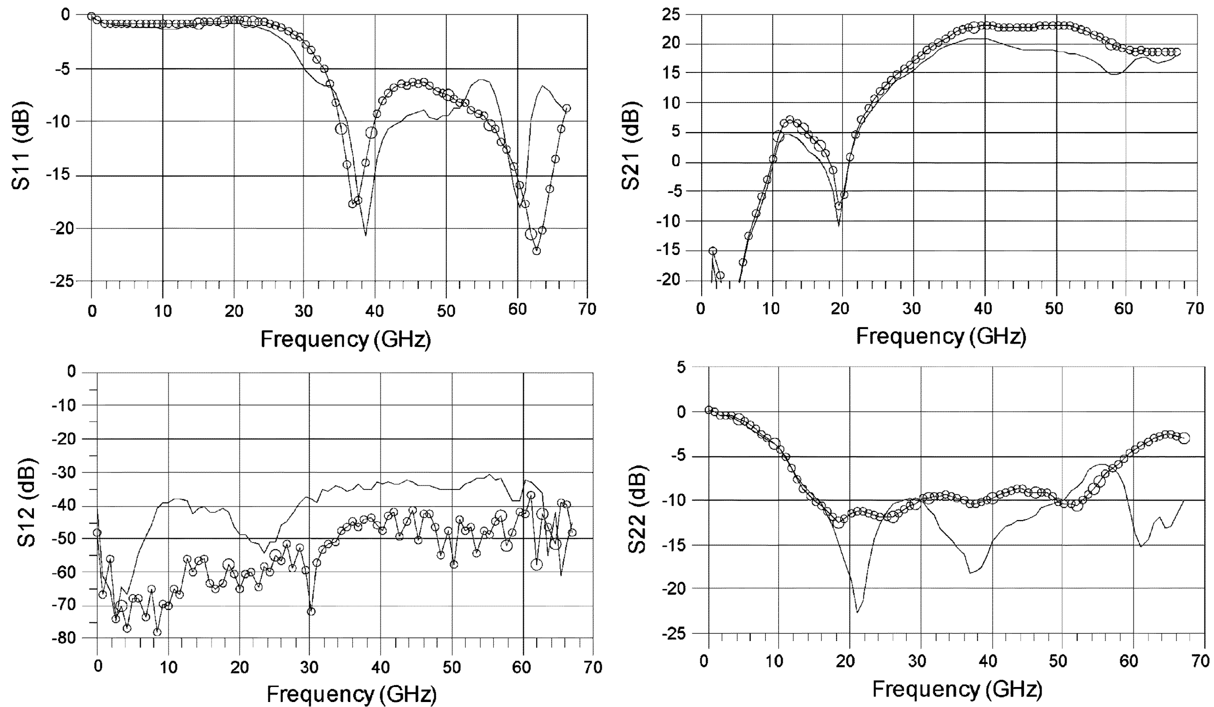


Fig. 18. Measured results of the amplifier before (o) and after (-) flip-chip assembly.

temperature co-fired ceramic (HTCC) [34], or even multi chip module deposited technology (MCM-D) [35]. Chip interconnects are provided by microstrip lines or co-planar waveguides (CPW). The interconnect loss is heavily dependent on the substrate material used. Ceramics are characterized by their low RF loss and good thermal properties but have a disadvantage of high cost. The inherent properties of ceramic material also implies that it cannot be formed into large sheet sizes like organic materials. However, lower-cost organic materials, such as epoxy-glass laminate (FR-4) and PTFE, have higher RF loss and worse thermal properties and are not frequently used at 60 GHz. The MMIC chips are connected to transmission lines using either conventional wire bonding or flip-chip assembly. Flip-chip assembly technologies have several advantages: compact size, low cost in large volumes, and excellent electrical performance (smaller parasitics compared to wire bonding) [36]. The excellent electrical performance concerns mainly the possibility to enhance the broadband performance compared to wire bonding. The bump transition itself is inherently broadband due to the very small parasitics of the bumps. However, problems with parasitic parallel plate modes may occur when microstrip MMICs are flip chip assembled, [37].

The three-stage small-signal MMIC amplifier used in this flip-chip test has more than 18 dB of gain between 32 and 67 GHz at a bias point of $V_G = -0.1$ V and $V_D = 1.7/2.45/2.45$ V for the first/second and third stage, respectively. The amplifier is a similar design to the three-stage amplifier presented in Section V.D.2 but the input stage is equipped with inductive feedback to lower the overall noise figure of the amplifier. The three-stage amplifier measures $3 \times 2$ mm$^2$ and a photo of the amplifier is found in Fig. 17 together with a photo of the flip-chip carrier. The carrier on which the MMIC later was mounted was designed in 254 $\mu$m thick alumina with etched gold pattern. The carrier has coplanar transmission lines with 50 $\Omega$ of characteristic impedance, i.e., the line width is 70 $\mu$m and the gaps are 40 $\mu$m. The total length of the carrier is 4.8 mm and it has no back side metallization.

To enable flip chip assembly, cylindrical pillars were electroplated on the thin film carrier. The pillars have a diameter of 75 $\mu$m and a height of 50 $\mu$m. The thermo compression flip chip bonding was made by the FC bonder PP5-TSV from JF Palomares. The chip was not heated itself but the carrier was heated to 300°C, the applied force was 35 grams per bump and the bond time was 15 seconds.

Two MMICs were assembled on carriers and measured in the same setup before and after the assembly with the same DC biases during all measurements. A 10 mm thick layer of rigid foam (Rohacell 31) was used during the measurements of the flip chip assembly as a distance washer between the grounded chuck of the probe station and the carrier. The rigid foam has a relative dielectric constant $(\varepsilon_r)$ of 1.04 and a loss tangent (tan $\delta$) of 0.011 at 26 GHz. Thus, the test device was moved away from the ground plane of the chuck and parallel plate modes did not occur. This measure to avoid parallel plate modes was also described in [38]. The 1.5 mm long transmission lines, at the input and output of the chip, adds approximately 0.7 dB extra loss at 60 GHz. This has not been taken into account when plotting the results from the assemblies with the on-chip measurement. The measurements show that the loss caused by the flip chip assembly is approximately 2–2.5 dB between 40 and 60 GHz when the loss in the coplanar transmission line on the substrate is subtracted, Fig. 18. This loss is mainly caused by thermal effects in the MMIC itself due to self-heating of the chip which degrades the performance of the amplifier. No mechanism for removing this heat was implemented during this test but special large thermal flip-chip bumps close to the devices could help to

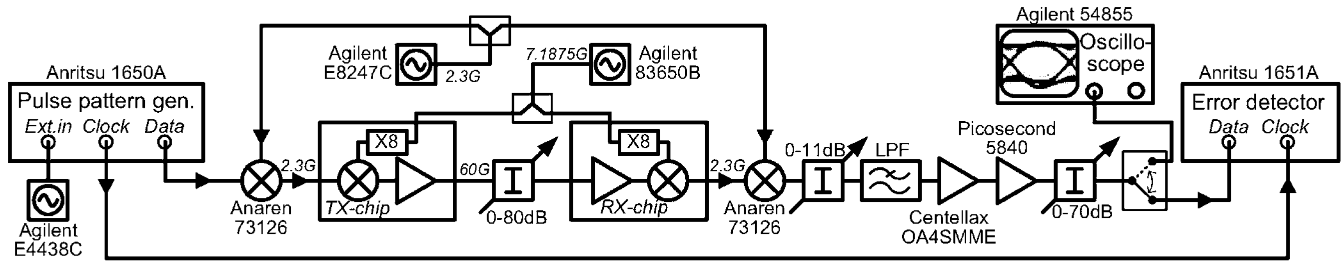


Fig. 19. Measurement setup used to test the maximum data rate capabilities of the transceiver chips.

reduce to self-heating and thus, improving the performance of the amplifier.

## IX. System-Level Measurements

The data transmission capabilities of the TX and RX chips were tested by transmission of a high speed ASK modulated digital signal. The setup used during these tests is illustrated in Fig. 19 and the measurement setup is described in detail below. The measurements in this section are complementary to the ones reported in [20]. In the earlier tests, we successfully transmitted and received QAM modulated signals using the first generation of the TX and RX MMICs. However, due to limitations in the used test setup, the maximum data rate was limited to a few hundred Mb/s. In the measurements described in this section, a low-order modulation format (ASK) is used, but the setup does not have the severe limitations in data rate as the previous system-level measurements. With the presented setup, both bit error rate (BER) and eye diagrams could be measured as a function of attenuation between the TX and RX MMICs, as well as the data rate.

### A. Measurement Setup

A pulse pattern generator (PPG) is used to provide a non-return to zero (NRZ) $2^{32}-1$ word length pseudo random binary sequence (PRBS) that is used as an input signal during the system tests. The data rate $(\mathrm{R_b})$, and thus the signal bandwidth, is controlled by an external sinusoidal source. The PPG baseband output signal is up converted to 2.3 GHz using a broadband double balanced mixer thus providing an IF input signal to the TX chip. The PPG output amplitude was adjusted to maximize the TX chip output power while maintaining acceptable nonlinear distortion level.

The TX and RX chips were placed in two separate probe stations during the measurements. A variable waveguide attenuator is connected between the chips to represent the path loss. The inherent high-pass nature of the waveguide section prevents signals below 50 GHz from leaking between the TX and RX chips.

A broadband mixer of the same type as used in the transmitter is used to down convert the IF output from the RX chip to baseband. The same LO sources feed both the transmitter and receiver mixers and MMICs and thus eliminate frequency drift problems. This eliminates the need for further receiver synchronization.

A low-pass filter is used in the RX baseband chain to lower the noise floor and thus increase the measurement dynamic range.

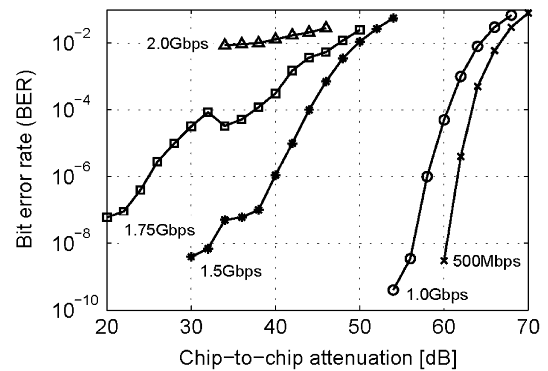


Fig. 20. Measured bit error rate (BER) versus chip-to-chip attenuation for different data rate settings.

Low-pass filters with different cutoff frequencies ranging from 600 MHz to 2.2 GHz were used depending on the $\mathrm{R_b}$ tested. Two cascaded broadband amplifiers providing in total 40 dB gain were used to increase the signal level as needed for the error detector (ED) instrument. The signal level was further controlled by two variable attenuators that simultaneously ensured that the amplifiers operated in a linear regime and that the ED operated with signal amplitude suitable for proper symbol detection.

Although the ED is synchronized to the PPG by a separate clock connection, the time delay through the system needs to be manually adjusted. This was done at each attenuator and $\mathrm{R_b}$ setting in order to obtain minimum BER results. The received signal quality was visually investigated by displaying eye diagrams on an oscilloscope that could replace the ED at the end of the receiver chain.

### B. Measurement Results and Discussion

The setup described above allows convenient testing of BER as function of $\mathrm{R_b}$ and chip-to-chip attenuation. The attenuation presented includes 11.4 dB total losses from cables, probes, and waveguide-to-coaxial transitions.

Fig. 20 shows BER versus attenuation for different $\mathrm{R_b}$ settings. The figure shows that 1.5 Gb/s can be transmitted through 47 dB attenuation with a raw BER $= 10^{-3}$, which is a typical requirement in wireless systems before adding error correction techniques. An idealized propagation calculation yields 88 dB free space path loss for 10 m transmission. Using directive antennas with approximately

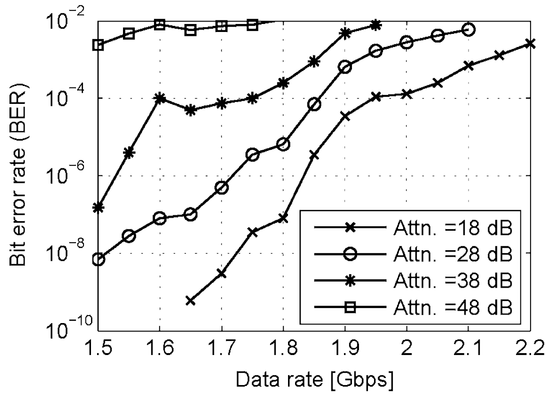


Fig. 21. Bit error rate (BER) versus data rate for different chip-to-chip attenuation.

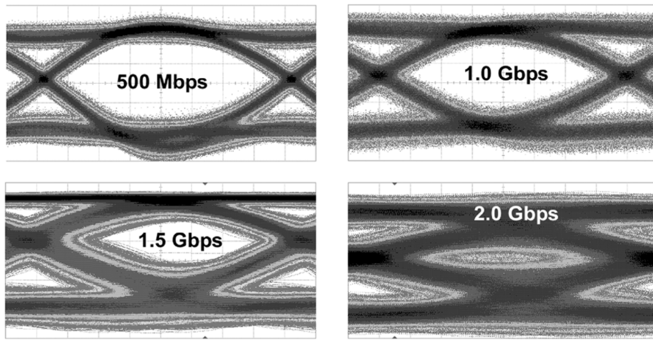


Fig. 22. Eye diagrams measured at the receiver for four different data rates.

20 dB gain each, this means that the chips developed would allow wireless communication up to 10 m at 1.5 Gb/s. However, much larger distances would be possible in real system using antennas with even higher directivity, more correct IF filtering, advanced modulation, and by introducing error correcting codes.

The maximum data rate is further explored in Fig. 21, which shows BER versus $R_b$ for four attenuation settings. This plot clearly shows that significantly higher data rates can be achieved if the path loss is decreased, either by using antennas with higher directivity, external power amplifier on the TX side, or shorter distance.

The received signal quality is illustrated in Fig. 22, which shows eye diagrams for $R_b$ ranging from 500 Mb/s to 2.0 Gb/s. Up to 1.5 Gb/s, the eye opening is reasonably well defined, which indicates low probability of error as presented in previous plots. At 2.0 Gb/s the eye has closed expressing the problem to communicate correctly at this data rate.

The test setup used is not well suited for evaluating wireless transmission using antennas since the chips are mounted in separate probe stations and use common LO sources. Nevertheless, some tests using 60 GHz horn antennas were performed and verified operation at 1.8 Gb/s up to 0.5 m with BER $< 10^{-3}$. The maximum distance was limited by the setup rather than the performance of the chips.

The RX/TX chip have an IF bandwidth of $>$ 1.8 GHz. The electrical 3 dB bandwidth typically needs to be at least 70% of $R_b$ for NRZ data, which would yield maximum $R_b >$ 2.6 Gb/s. However, in the present system $R_b$ is probably limited by group delay variations and receiver noise rather than the electrical bandwidth itself. For example, no external bandpass filter is used in front of the RX chip, which significantly increases the receiver noise level and degrades the dynamic range. The external baseband-to-IF mixers used have an electrical bandwidth of 1.5 GHz, which should also degrade the performance at high $R_b$, although they were tested separately and allowed error free operation up to 2 Gb/s. Further investigations will address performance limiting factors in the presented TX and RX MMICs.

## X. Comparison With the Work of Others

Table I and II gives a comparison of the presented mHEMT MMICs with other silicon-based multifunctional transmitter and/or receiver mm-wave MMICs presented in the open literature. The comparison has been made with a special focus corresponding transmitter and/or receiver MMICs in silicon technologies since GaAs based multifunctional MMICs are rare and most research activities in this area are focused on silicon. Table I gives an overview of the integrated functionality of every MMIC and Table II gives some key data in order to compare the different designs. To the best of the authors' knowledge, Table I and II contain all existing multifunctional transmitter and/or receiver mm-wave MMICs implemented in silicon technologies and presented in the open literature. It is difficult to make a fair comparison between the different designs since they are aimed for different purposes.

From Table I, it can be concluded that the silicon designs often contains a VCO and in many cases also a PLL. This would indeed have been possible in a GaAs HEMT design as well since a single chip V-band PLL has been demonstrated in a GaAs pHEMT technology [39]. The reason why neither a VCO nor a PLL was integrated in the mHEMT MMICs presented in this paper was that the MMICs were intended to be used for many different applications, and hence, many different requirements on the phase noise and settling time for the PLL would have set up contradictory goals for that part of the design.

It can also be concluded that the presented mHEMT MMICs are the only MMICs that contains an integrated IF hybrid and/or balun. This was chosen to simplify the use of the MMICs as direct frequency up/down converters with a minimum of external passive components. However, in some applications such as the 77 GHz transmitter and receiver intended for automotive radar reported in [16] and [17], a quadrature input/output baseband signal may be more convenient from a system perspective.

The moderate TX output power and RX noise figure of the presented mHEMT MMICs compared to best values of the comparative silicon MMICs is explained by the fact that the same three-stage amplifier was used as both a post-amplifier in the TX and a LNA in the RX MMICs. This three-stage amplifier was mainly designed for broad bandwidth and flat gain rather than high power or low noise.

Contradictory to the presented mHEMT MMICs, many of the silicon designs utilizes balanced designs throughout the TX or RX. The presented mHEMT MMICs are instead single-ended designs to reduce the DC power consumption and save chip area (and thus, also reducing the cost).

TABLE I
COMPARISON OF INTEGRATED FUNCTIONALTY

| | Oper. freq (GHz) | Comment | MMIC technology | PA | LNA | Up and/or down conv. mixer | Single/dual stage freq. conversion | IF hybrid/ /balun | IF amp. | LO hybrid/ /balun | Mult. order of ev. LO chain | VCO | PLL | Integ. antenna |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| This work | 60 | Multfunctional TX/RX | 0.15 μm GaAs mHEMT | X | X | X | single | X | | X | X8 | | | |
| [20] | 60 | Multfunctional TX/RX | 0.15 μm GaAs pHEMT | X | X | X | single | X | | X | X8 | | | |
| [12] | 60 | Multfunctional TX/RX | 0.13 μm SiGe BiCMOS | X | X | X | dual | | X | | X3 | X | X | |
| [13] | 60 | Multfunctional TX | 0.18 μm SiGe BiCMOS | X | | X | single | | | | | X | | X |
| [14] | 60 | Multfunctional RX | 0.13 μm CMOS | | X | X | single | | | | | | | |
| [15] | 60 | Multfunctional RX | 0.13 μm CMOS | | X | X | single | | X | | | | | |
| [16-17] | 77 | Multfunctional TX/RX | 0.12 μm SiGe BiCMOS | X | X | X | dual | | X | | | X | X | X |
| [18] | 24 | Multfunctional RX | 0.18 μm SiGe BiCMOS | | X | X | dual | | X | | | X | X | |
| [19] | 24 | Multfunctional TX | 0.18 μm CMOS | X | | X | dual | | X | | | X | X | |

TABLE II
COMPARISON OF KEY DATA

| | Oper. freq (GHz) | Comment | MMIC technology | TX gain (dB) | RX gain (dB) | TX output power (dBm) | RX NF (dB) | RX image rejection ratio (dB) | RX $CP_{1dB}$ (dBm) | RX IIP3 (dBm) | Input LO freq. (GHz) | IF freq. (GHz) | TX DC power cons. (mW) | RX DC power cons. (mW) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| This work | 60 | Multfunctional TX/RX | 0.15 μm GaAs mHEMT | 0.6 | 12.9 | 5.6 | 7.2 | 14.6 | -17 | -10 | 7.1875 | 2.5 | 420 | 450 |
| [20] | 60 | Multfunctional TX/RX | 0.15 μm GaAs pHEMT | 5.2 | 8.5 | 3.3 | 9.8 | 27.6 | -19 | -11 | 7.1875 | 2.5 | 820 | 990 |
| [12] | 60 | Multfunctional TX/RX | 0.13 μm SiGe BiCMOS | 37 | 39.8 | 17 | 6 | > 30 | -36 | -30 | On-chip VCO | $\approx$0 (BB) | 510 | 530 |
| [13] | 60 | Multfunctional TX | 0.18 μm SiGe BiCMOS | 20.2 | | 15.8 | | | | | On-chip VCO | $\approx$0 (BB) | 281 | |
| [14] | 60 | Multfunctional RX | 0.13 μm CMOS | | 24 | | 10.5 | | -11 | | 60 | $\approx$0 (BB) | | 8.6 |
| [15] | 60 | Multfunctional RX | 0.13 μm CMOS | | 27.5 | | 12.5 | | -22.5 | | 60 | $\approx$0 (BB) | | 9 |
| [16-17] | 77 | Multfunctional TX/RX | 0.12 μm SiGe BiCMOS | 40.6 | 31 | 12.5 | | | | | On-chip VCO | $\approx$0 (BB) | 730 | |
| [18] | 24 | Multfunctional RX | 0.18 μm SiGe BiCMOS | | 43 | | 7.4 | 35 | -27 | -11.5 | On-chip VCO | $\approx$0 (BB) | | |
| [19] | 24 | Multfunctional TX | 0.18 μm CMOS | | | 14 | | | | | On-chip VCO | $\approx$0 (BB) | 770* | |

*One signal path + VCO + PLL

Besides from the different designs presented in Table I and II, there exists also a number of presented TX and RX modules where individual GaAs based MMICs (amplifiers, mixers, multipliers, etc.) are bonded on a common substrate [7]–[9]. The main activity in this field has been in Japan where companies such as NEC even have integrated such module into a fully functioning Gigabit Ethernet transceiver with optical input and demonstrated transmission and reception of data rates up to 1.25 Gb/s, [10]. However, the presented single-chip mHEMT TX and RX MMICs could lower the cost for such a system significantly. The main cost reduction from using single-chip TX and RX MMICs instead of a solution with several MMICs origins from substantially reduced cost for packaging and maintenance (replacing broken MMICs, etc.) of the mm-wave unit due to the many MMICs involved. Furthermore, unlike many of those presented chip-sets and modules who are designed for binary modulation only, the mHEMT TX and RX MMICs presented in this paper are capable of using any kind of modulation, thus representing a much more flexible solution.

## XI. SUMMARY AND DISCUSSION

The measured performance of the presented TX and RX chips are in detail summarized in Tables III and IV, respectively. The default values for RF, LO, and IF frequencies have been 60 GHz,

TABLE III
SUMMARY OF MEASURED RESULTS FOR THE TX CHIP

| Conversion Gain, dB | Output power (dBm) | 3 dB RF BW (rel. $f_C$), GHz | 3 dB IF BW (rel. $f_C$), GHz |
|---|---|---|---|
| 0.6 | 5.6 | 8 (56.5 – 64.5) | 1.8 (1.9 - 3.7) |

| 1dB Input Comp. Point, dBm | LO Power, dBm | Power Cons. (mW) |
|---|---|---|
| -1 | -3 | 420 |

TABLE IV
SUMMARY OF MEASURED RESULTS FOR THE RX CHIP

| Conversion Gain, dB | 3 dB RF BW (rel. $f_C$), GHz | 3 dB IF BW* (rel. $f_C$), GHz | Image Rejection Ratio (dB) |
|---|---|---|---|
| 12.9 | 10 (54.5 – 64.5) | 1.9 (1.3 - 3.2) | > 13 (57.5 - 67.5 GHz) |

| 1dB Input Comp. Point, dBm | IIP3, dBm | LO Power, dBm | Noise Figure, dB | Power Cons. (mW) |
|---|---|---|---|---|
| -17 | -10 | -2 | 7.2 | 450 |

*And a IRR of more than 10 dB

7.1875 GHz (giving 57.5 GHz output frequency from the X8), and 2.5 GHz, respectively.

The presented TX and RX chips are true multipurpose 60 GHz front-end designs. During the measurements, the DC bias was adjusted to find the optimal performance at 60 GHz in terms of output power for the TX chip and conversion gain for the RX chip. Compared to the first generation of the designs, [20], the MMICs presented in this paper show the same high level of integration but occupy smaller chip area and have higher gain and output power at only half of the DC power consumption. The reduction in DC power consumption was obtained by optimizing the overall design with respect to DC power consumption, e.g., the number of stages in the buffer amplifier used in the X8 LO multiplier chain was reduced from two to one stage compared with the pHEMT TX and RX MMICs. Furthermore, the higher transconductance $(g_m)$ in the mHEMT compared to its pHEMT counterpart made it possible to use lower drain biases (and hence reduced DC power consumption) in the former for the same mode of operation.

Although only a small number of chips have been measured, i.e., less than five TX and RX chips, no malfunctioning chips have been found and the yield is therefore expected to be good.

Different packaging and interconnects issues were also presented. As an alternative to wire bonding, experimental results of amplifiers mounted with flip-chip assembly technique were also presented. The flip-chip interconnection added 2–2.5 dB of loss between 40 and 60 GHz compared to when the amplifiers were measured directly on-chip with coplanar GSG probes.

Finally, system measurements are described where the presented TX and RX MMICs successfully transmitted and received a modulated signal. The system measurements in this paper are complementary to the ones reported in [20]. In the earlier tests, we successfully transmitted and received QAM modulated signals using the first version of the TX and RX MMICs. However, due to limitations in the used test setup, the maximum data rate was limited to a few hundred Mb/s. In the measurements described in this paper, a low-order modulation format (ASK) is used, but the setup does not have the severe limitations in data rate as the previously reported system-level measurements. Plots of bit error rate (BER) versus attenuation between the TX and RX MMICs together with eye diagrams have demonstrated that the presented TX and RX MMICs support data rates beyond 1.5 Gb/s, even when using very simple ASK modulation.

## XII. CONCLUSION

The 60 GHz MMIC transmitter and receiver chips, designed in an mHEMT technology, have been simulated, manufactured, and experimentally verified. The single chip transmitter MMIC consists of a balanced resistive mixer with an integrated ultra broadband IF balun, a three-stage post amplifier, and a multiply-by-eight (X8) LO multiplier chain. The single chip receiver MMIC has an equally high level of integration with a three-stage low noise amplifier, an image reject mixer with an integrated ultra broadband IF hybrid and the same X8 LO multiplier chain as used in the transmitter chip.

Packaging and interconnects are discussed and as an alternative to wire bonding, flip-chip assembly tests were also presented and discussed. The results clearly showed the suitability of flip-chip as a broadband interconnecting technique for MMICs.

The system-level measurements of BER and eye diagrams have demonstrated that the presented TX and RX MMICs support data rates beyond 1.5 Gb/s, even using a simple ASK modulation. Using higher order modulation (e.g., QPSK or QAM), more correct IF filtering, and by introducing error correcting codes the maximum data rate could be extended even further.

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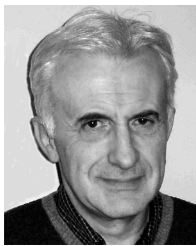

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