6.2 A SAW-Less Multiband WEDGE Receiver

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With an ever-increasing number of frequency bands supported by cellular transceivers (TRX), front-end (FE) complexity increases due to a large number of external SAW filters. The challenge of removing inter-stage filters from the baseband (BB) path leads to the removal of the additional noise contribution due to limited transmitter (TX) leakage rejection at the RX input, inputmodulation (IM) products and cross-compression due to TX leakage and strong out-of-band blockers. Increased downconverter dynamic range is thus required for a SAW-less RX path. In addition, avoiding SNR degradation from reciprocal mixing imposes additional constraints on LO phase noise.

The presented transceiver (Fig. 6.2.1) integrates all RX and TX functions required to support a tri-band WCDMA/HSPA (bands I-VI, VIII, IX) and quad-band GSM/EDGE application in a single chip. The TX circuit employs a 2-metal passive integration technology (PICS) allowing the integration of high-Q LNA degeneration inductors, TX matching networks, PLL filters and high-density supply-decoupling capacitors. The active die (10 mm²) and passive (40 mm²) die are double-flip-chip mounted into a 56-pin QFN and the TRX components, including supply decoupling into a single package. A crystal resonator is the only external component. The VCOs employ octagonal-shaped coils (Q ~19 at 4GHz) to mitigate external feedback. The TX leakage rejection at the RX input is limited to 95dB, and TX VCOs, RX input and TX output paths are routed orthogonal to further minimize the RF coupling.

The baseband channel filter (BCF) (Fig. 6.2.3) is designed as a reconfigurable Legendre 5th-order (Gain~63 to 65dB, BW~2.15MHz) response filter in WCDMA mode and a Butterworth 3rd-order (Gain~25 to 28dB, BW~230kHz) response in GSM/EDGE mode. The BCF helps to overcome process and temperature drifts. The 3rd-order PLL filters and high-density supply-decoupling capacitors. The active die (10mm²) and passive (40mm²) die are double-flip-chip mounted into a 56-pin QFN package. In order to improve the isolation between RX and TX paths (operating simultaneously in 3G mode), octagonal-shaped VCO inductors are used with mutually-orthogonal orientations to achieve better than 95dB isolation between RX and TX VCOs. RX input and TX output paths are routed orthogonal to further minimize the RF coupling.

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Figure 6.2.2 shows the FE architecture, comprising seven single-ended gain-switchable LNAs (three in 3G and four in 2G). A dual-core structure provides high isolation between input and minimum group-delay and change when switching between high and low gain (16dB) modes. The LNA generation inductors are implemented in Al-metal on the passive substrate (PICS), with typical inductance/Q-factor values of 0.7nH/20 at 2GHz and 2.3nH/18 at 1GHz. In 2G mode, each pair of high/low-band LNAs employs a shared degeneration inductor to save area. The LNA output currents are combined in a 2x2-level cascode circuit and passed through to the RX balun primary coil. Large PMOS devices are used to configure this inductance between low- and high-band settings, with transfer ratios of 6/4:3 in high/low band, respectively. The interstage frequency response is tuned per band using a capacitance DAC. The LNA output-current signal is AC coupled to the downconverter core via the balun and 3G RF receiver (RX) resides in the additional noise biasing of the downconverter core. The balun output current circulates through two identical current components, consisting of transistors Q1, Q1′, Q1′′, Q2′, Q2′′, respectively. In high-band operation, the overall current-consumption sequence is generated by directing the CK+ controlled, VCO-rate current pulses through CK- to the baseband outputs via CK2-rate switches Q2, Q′2. Sequencing signals L1, L2, L3, L4 are generated by a conventional divide-by-2 quadrature circuit. The switching transistors of Q2, Q′2 are controlled such that the sequencing signals are stable for the duration of the corresponding CK half-period. In this way, sequence output jitter is masked and low-power operation is possible without impact on reciprocal mixing of out-of-band blockers.

As a result, Q1 RF input current is directed to the I+, Q-, I-, Q+ outputs for sub-sequent quarters of the CK2 signal period. Conversion gain is v2x2a for each of the differential baseband outputs. Due to signal current re-use in the second commutator, overall conversion gain is v2x4n, 32dB higher than for a traditional Gilbert I/Q-mixer having the same current consumption. I/Q gain and phase balance are achieved by maintaining accurate 50% duty cycle throughout the VCO paths, and converter IP2 is maximized by maintaining a high degree of active and passive component matching. Out-of-band blocking is maximized by protecting the baseband filter via a tuned RC roofing filter pole.

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Figure 6.2.5 shows measured RX Noise Figure (NF) results for two scenarios in band II (1900MHz):

1) in the presence of a WCDMA modulated blocking signal generated by the on-chip TX at the band-specific duplex offset frequency (80MHz)
2) in the presence of a -45dBm CW blocking signal at half and double duplex offset frequencies (respective to a -15dBm blocker at the antenna and 30dB blocker attenuation).

Cross-compression, IM2 and IM3 performances are shown with CW, WCDMA TX, and WCDMA TX & CW blockers respectively. Under worst-case duplex TX-RX isolation, a -26dBm out-of-band blocker at the LNA input results in 2.7dB/3dB NF, under CW and WCDMA modulation respectively. Desensitization due to -26dBm CW blockers in addition to TX leakage is:

- 0.5/1.7dB at -380/-95MHz offset, respectively (band I)
- 0.6/1.8dB at -160/-40MHz offset, respectively (band II)
- 1/2dB at -90/-22.5MHz offset, respectively (band V)

Figure 6.2.4 shows measured RX EVM for 3GPP test-model 5 HSDPA with 16-QAM modulation. A low EVM of less than 6% is maintained over a wide input power range. Figure 6.2.6 shows a comparison with published RX work [2, 3].

A significant contribution to overall WEDGE radio cost is due to phone production. In this TRX, all filters, VCOs and PLL bandwidths are internally self-calibrated.

The active die is implemented in a 0.25µm BiCMOS process. The carrier sub-strate is realized in PICS and integrates all TX components, including supply de-coupling into a single package. A crystal resonator is the only external component required. This TRX is in volume production.

References:
Figure 6.2.1: Multi-band WEDGE transceiver block diagram.

Figure 6.2.2: WEDGE RX front-end schematic.

Figure 6.2.3: WEDGE RX baseband filter and AGC schematic.

Figure 6.2.4: Out-of-band IIP2 and RX EVM (3GPP test-model 5&8 HS-PDSCH) versus input power.

Figure 6.2.5: WCDMA Band II NF versus frequency and versus TX Power at LNA.

Figure 6.2.6: Receiver performance summary.
Figure 6.2.7: Transceiver micrograph highlighting the receiver path.